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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hisashi Ohtani, et al. Art Unit : 2815
Serial No.: 09/379,702 Examiner : Eugene Lee
Filed : August 24, 1999
Title : METHOD OF FABRICATING SEMICONDUCTOR DEVICES

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T. Flaeger

Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF ENGLISH TRANSLATION

Pursuant to 37 CFR 1.55(a) and in accordance with the amendment dated April 12, 2001, enclosed herewith is an English translation of Japanese specification no. 7-338130, filed November 30, 1995, for the above-identified patent application and the executed verification of translation.

Please apply any charges or credits to our Deposit Account No. 06-1050.

Respectfully submitted,

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Attorney Docket No. 07977/093002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.: 09/379,702 Group Art Unit: 2815
Filed: August 24, 1999 Examiner: LEE, E
Title: METHOD OF FABRICATING SEMICONDUCTOR DEVICES

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Ikuko Noda, 3-G, 1551, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 7-338130 filed on November 30, 1995; and

that to the best of my knowledge and belief the following is a true and correct translation of the Japanese Patent Application No. 7-338130 filed on November 30, 1995.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 25th day of April, 2001

Ikuko Noda

Name: Ikuko Noda

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[Attachment]	Specification 1
[Attachment]	Drawing 1
[Attachment]	Abstract 1

[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION] Method of fabricating semiconductor device

[WHAT IS CLAIMED IS:]

1. A method of fabricating a semiconductor device having a step of crystallizing an amorphous silicon film formed on an insulating substrate by a catalytic action of a metal element, comprising the steps of:

forming a first insulating film on said amorphous silicon film;

forming holes in said insulating film to selectively expose a surface of said amorphous silicon film;

introducing said metal element into said amorphous silicon film from the exposed surface;

crystallizing said amorphous silicon film to form a crystalline silicon film;

etching said crystalline silicon film into an island while leaving said insulating film on said crystalline silicon film to form an active layer; and

forming a second insulating film.

2. A method of fabricating a semiconductor device having a step of crystallizing an amorphous silicon film formed on an insulating substrate by a catalytic action of a metal element, comprising the steps of:

forming a first insulating film on said amorphous silicon film;

forming holes in said insulating film to selectively expose a surface of said amorphous silicon film;

introducing said metal element into said amorphous silicon film from the exposed surface;

crystallizing said amorphous silicon film to form a crystalline silicon film;

removing a surface of said first insulating film heavily doped with said metal element;

etching said crystalline silicon film into an island while leaving said insulating film on said crystalline silicon film to form an active layer; and

forming a second insulating film.

3. The method of claim 1 or claim 2, wherein said first insulating film is made of silicon oxide film.

4. The method of claim 1 or 2, wherein said first insulating film is made of silicon nitride film.

5. The method of claim 1 or claim 2, wherein said step of forming said first insulating film involves a step of forming silicon oxide at least at an interface between said first insulating film and said amorphous silicon film by thermal oxidation.

6. The method of claim 1 or claim 2, wherein said second insulating film is made of silicon oxide.

7. The method of claim 1 or claim 2, wherein said second insulating film is made of silicon nitride.

8. The method of claim 1 or claim 7, wherein one or more elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au are used as said metal element.

9. A method of fabricating semiconductor devices having a step of crystallizing an amorphous silicon film formed on an insulating substrate by a catalytic action of a metal element, comprising the steps of:

forming a first insulating film on said amorphous silicon film;

forming holes in said insulating film to selectively expose a surface of said amorphous silicon film;

introducing said metal element into said amorphous silicon film from said exposed surface;

crystallizing said amorphous silicon film to form a crystalline silicon film;

illuminating said crystalline silicon film with laser light;

etching said crystalline silicon film into an island while leaving said insulating film on said crystalline silicon film to form an active layer; and

forming a second insulating film.

10. A method of fabricating semiconductor devices having a step of crystallizing an amorphous silicon film formed on an insulating substrate by a catalytic action of a metal element, comprising the steps of:

forming a first insulating film on said amorphous silicon film;

forming holes in said insulating film to selectively expose a surface of said amorphous silicon film;

introducing said metal element into said amorphous silicon film from said exposed surface;

crystallizing said amorphous silicon film to form a crystalline silicon film;

illuminating said crystalline silicon film with laser light;

etching said crystalline silicon film into an island while leaving said insulating film on said crystalline silicon film to form an active layer; and

forming a second insulating film,

wherein said first insulating film is reduced to a thickness sufficient to act as an antireflective film for said laser light having a given wavelength.

11. A method of fabricating a semiconductor device having a step of forming an active layer made of a crystalline silicon film, on an insulating substrate and a step of forming a gate insulating film on a surface of said active layer, comprising the steps of:

forming a first insulating film constituting a bottom layer of said gate insulating film, on said amorphous silicon film;

forming holes in said insulating film to selectively expose a surface of said amorphous silicon film;

introducing said metal element into said amorphous silicon film from said exposed surface;

crystallizing said amorphous silicon film to form a crystalline silicon film;

illuminating said crystalline silicon film with laser light;

etching said crystalline silicon film into islands while leaving said insulating film on said crystalline silicon film to form an active layer; and

forming a second insulating film,

wherein said gate insulating film comprises a laminate film of said first insulating film and said second insulating film,

wherein the thickness of said first insulating film is not larger than that of said gate insulating film and is so controlled that the film acts as an antireflective film for the wavelength of said laser.

12. The method of claims 9 to 11, wherein said laser is emitted by a KrF excimer laser, and wherein said first insulating film is made of silicon oxide and has a thickness of 300 to 600 Å.

13. The method of claims 9 to 11, wherein said laser light is emitted by a KrF excimer laser,

and wherein said first insulating film is made of silicon nitride and has a thickness of 250 to 500 Å.

14. The method of claims 9 to 11, wherein said laser light is emitted by an XeCl excimer laser, and wherein said first insulating film is made of silicon oxide and has a thickness of 400 to 700 Å.

15. The method of claims 9 to 11, wherein said laser light is emitted by an XeCl excimer laser, and wherein said first insulating film is made of silicon nitride and has a thickness of 350 to 600 Å.

16. The method of claims 9 to 11, wherein during said step of forming said insulating films, silicon oxide is formed at least at an interface with said amorphous silicon film by thermal oxidation.

17. The method of claims 9 to 11, wherein one or more elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au is used as said metal element.

18. A method of fabricating a semiconductor device having a step of crystallizing an amorphous silicon film formed on an insulating substrate by a catalytic action of a metal element, comprising the steps of:

forming a first insulating film on said amorphous silicon film;

forming holes in said insulating film to selectively expose a surface of said amorphous silicon film;

introducing said metal element into said amorphous silicon film from the exposed surface;

crystallizing said amorphous silicon film to form a crystalline silicon film;

removing a surface of said first insulating film heavily doped with said metal element;

irradiating said crystalline silicon film with laser;

etching said crystalline silicon film into an island while leaving said insulating film on said crystalline silicon film to form an active layer; and

forming a second insulating film.

19. A method of fabricating a semiconductor device having a step of crystallizing an amorphous silicon film formed on an insulating substrate by a catalytic action of a metal

element, comprising the steps of:

forming a first insulating film on said amorphous silicon film;

forming holes in said insulating film to selectively expose a surface of said amorphous silicon film;

introducing said metal element into said amorphous silicon film from the exposed surface;

crystallizing said amorphous silicon film to form a crystalline silicon film;

irradiating said crystalline silicon film with laser;

removing a surface of said first insulating film heavily doped with said metal element;

etching said crystalline silicon film into an island while leaving said insulating film on said crystalline silicon film to form an active layer; and

forming a second insulating film,

wherein the thickness of said first insulating film is so controlled that the film acts as an antireflective film for the wavelength of said laser.

20. The method of claim 18 or claim 19, wherein one or more elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au is used as said metal element.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a method of fabricating a semiconductor device by using thin-film transistors (TFTs) or the like, and more particularly, to a method of fabricating a semiconductor device using a crystalline silicon film which is crystallized by the catalytic action of a metal element.

[0002]

[Prior Art]

In recent years, a constitution in which thin film transistors are used for a liquid crystal device has attracted attention. This is known as an active matrix liquid crystal display and has millions of pixels arranged in rows and columns. TFTs are connected with each pixel. This liquid crystal display is characterized in that the manner in which electric charge is stored in pixels and transmitted out of them is controlled by these TFTs. This active matrix liquid crystal display is capable of providing a fine display at a high speed. Consequently, the active matrix liquid crystal display is used in displays of portable word processors and computers.

[0003]

Although an amorphous silicon film is conveniently used as a silicon film incorporated in TFTs, the electrical characteristics of the amorphous silicon film are inferior than those of single-crystal semiconductor used in a semiconductor integrated circuit. Therefore, TFTs using the amorphous silicon film can be used only in limited applications such as switching elements in active matrix circuits.

[0004]

In order to improve the characteristics of a TFT, a silicon film having crystallinity may be used. Besides single-crystal silicon, a polycrystalline silicon film and a micro-crystallite silicon film are known as silicon films having crystallinity. In order to obtain such a silicon film having crystallinity, an amorphous silicon film is formed and then heated by thermal annealing to crystallize the amorphous film. This method is known as a solid phase growth method, because the crystal state is changed from amorphous state to crystalline state while the solid phase is maintained.

[0005]

Generally, liquid crystal displays are required to use substrates having transparency and so limitations are imposed on the substrate material. Generally, glass is only a material which satisfies the conditions such that it has transparency, it is not expensive, and it is provided with a large area.

[0006]

Where silicon is grown by solid phase growth, the heating temperature is 600°C or higher and the heating time is not less than 10 hours. Corning 7059 glass which is widely accepted into general use has a strain point of 593°C. Where increases in area of substrates are taken into account, it is difficult to perform thermal annealing at 600°C or higher.

[0007]

[Problems to be solved by the Invention]

[Process leading to the Invention]

In view of these problems, the present inventors conducted researches. It was clarified that if a trace amount of a metal element is added to an amorphous silicon film, crystallization of silicon is promoted by the catalytic action of the metal element, and that the crystallization temperature can be lowered and the crystallization time can be shortened. More specifically, it was discovered that silicon can be crystallized by performing a heat-treatment at 550°C for about 4 hours. Therefore, TFTs using a crystalline silicon film can be fabricated on a glass substrate.

[0008]

One or more elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au can be appropriately selected as the aforementioned metal element having catalytic action. Among them, nickel (Ni) produces especially conspicuous crystallization effect.

[0009]

Methods for introducing metal elements into an amorphous silicon film include (i) a method consisting of bringing a coating, particles, clusters, or the like including a metal element into intimate contact with an amorphous silicon film, (ii) a method of consisting of applying an aqueous solution containing a metal element, and (iii) an ion implantation method. An amorphous silicon film in which a metal element has been introduced is crystallized by heating the film at a temperature of 450-580°C for 4 to 8 hours.

[0010]

According to the research by the present inventors, in the crystallization process of silicon where a metal element is added, heating causes amorphous silicon to react with the metal element, thus forming silicide. Then, silicon is heteroepitaxially grown on the surface of the silicide which acts as nuclei. The dimensions of nuclei of silicide depend on thermal factors, the thickness of the amorphous silicon, and other factors. Where nickel is used as a metal element, the dimensions are on the order of 500-2000 Å. Therefore, obtained silicon crystals are columnar-shaped crystals having widths comparable to those of the nuclei. The crystals grow from regions in which the metal element has been introduced toward the surroundings. Consequently, the crystal growth can be controlled by controlling the regions in which the metal element is introduced and their shapes.

[0011]

Fig. 6 illustrates an explanatory drawing of crystallization processes of silicon, utilizing the catalytic action of a metal element, which has been conventionally disclosed by the present inventors. As shown in Fig. 6(A), a base film 12 comprising silicon oxide and an amorphous silicon film 13 are formed on a glass substrate 11.

[0012]

Then, a silicon oxide film 14 is formed to a thickness of 500 to 2000 Å, thereby a hole 14a is formed. Typically, the hole 14a takes a rectangular form extending in a direction vertical to the plane of the figure.

[0013]

In the hole 14a, a thin oxide film (not shown) is formed on the surface of the amorphous

silicon film 13 to a thickness of about 10 to 50 Å. This thin oxide film improves the surface characteristics of the amorphous silicon film 13 and thus the amorphous silicon film no longer repels aqueous solution. The thin oxide film can be formed by ultraviolet radiation within an oxygen atmosphere or immersing the substrate in ozone water or hydrogen peroxide water.
[0014]

In order to introduce nickel, which is a metal element for promoting crystallization of silicon, into the amorphous silicon film 13 under this condition, aqueous solution of nickel acetate is applied by spin coating and dried. As a result, an extremely thin nickel film 15 is formed in intimate contact with the surface of the amorphous silicon film 13 in the hole 14a of the silicon oxide film 14.
[0015]

As shown in Fig. 6(B), after removing the silicon oxide film 14, a heat treatment is performed at a temperature of 450 to 640°C for 4 to 8 hours, typically at 550°C for 8 hours. Crystals are grown from the regions with which the extremely thin nickel film 15 is in contact in directions parallel to the substrate 11 indicated by the arrows. As a result, a crystalline silicon film 16 is formed. The crystal growth distance can be set to several tens of micrometers to 100 μm or more. Where a glass substrate is used as the substrate, the heating temperature is preferably set not higher than the strain point of the glass substrate in order to prevent the glass substrate from shrinking or deforming.
[0016]

As shown in Fig. 6(C), after the crystal growth, the silicon oxide film 14 is removed. Thereafter, if necessary, laser annealing may be performed to improve the crystallinity of the crystalline silicon film 16. This crystalline silicon film 16 has a region 16a located immediately under the thin nickel film 15. In this region 16a, crystals are grown vertical to the glass substrate 11. The crystallographic axis is not uniform. This growth is referred to as vertical growth. On the other hand, in a region 16b located in the periphery of the vertical growth region 16a, crystals are grown parallel to the glass substrate 11 with a substantially uniform crystallographic axis. This crystal growth is referred to as lateral growth.
[0017]

As shown in Fig. 6(D), the crystalline silicon film 16 is patterned to form an active layer 17 for TFTs. A silicon oxide film 18 acting as a gate-insulating film is formed. The TFTs are completed by well-known fabrication techniques. The region located just under the extremely thin nickel film 15 and the regions in which the crystal growth terminates are heavily doped with nickel and so it is necessary that these regions be not contained in the channel formation

region.

[0018]

Silicon crystals can be grown parallel to the substrate 11, i.e., laterally, as shown in Fig. 6(B), by adopting the above-described crystallization techniques. Since the directions of crystals of the obtained crystalline silicon film 16 are uniform, TFTs using this crystalline silicon film 16 show good electrical characteristics and are capable of operating at high speed.

[0019]

In the above-described crystallization step, however, after obtaining the crystalline silicon film 16, the mask 14 is removed, and the surface of the crystalline silicon film 16 is exposed. Therefore, there is the possibility that the surface is contaminated. Furthermore, ridges might be formed because the laser annealing is carried out while the surface of the crystalline silicon film 16 is exposed. The contamination and the ridges will raise the interface level between the active layer 17 and the gate-insulating film. Hence, the characteristics of the TFTs are deteriorated.

[0020]

It is an object of the present invention to provide a method of fabricating semiconductor devices having good interface levels of the active layer by solving the foregoing problems.

[0021]

[Means to solve the Problems]

In order to solve the foregoing problems, a semiconductor device fabrication method according to the present invention comprises the steps of: forming a first insulating film on said amorphous silicon film; forming holes in the insulating film to selectively expose a surface of said amorphous silicon film; introducing said metal element into the amorphous silicon film from the exposed surface by the step; crystallizing the amorphous silicon film to form a crystalline silicon film; etching the crystalline silicon film together with the first insulating film to form an active layer; and forming a second insulating film.

[0022]

In the method of fabricating semiconductor devices having the above means, the amorphous silicon film formed on the insulating substrate is crystallized by making use of catalytic action of the metal element. In this step, the metal element is selectively introduced into the amorphous silicon film. For this purpose, the first insulating film is used as a barrier film. The holes are selectively formed in the first insulating film to partially expose the surface of the amorphous silicon film.

[0023]

The step of introducing the metal element into the amorphous silicon film can utilize a step of applying a solution containing the metal element to the amorphous silicon film. The use of the solution facilitates controlling the concentration of the metal element in the amorphous silicon film. Furthermore, the metal element can be retained in contact with the amorphous silicon film uniformly.

[0024]

In order to crystallize the silicon by heat-treatment, it is necessary to introduce the metal element into the amorphous silicon film at a concentration of 1×10^{16} cm^{-3} or more. However, if the metal element is introduced in the amorphous silicon film at a concentration of 5×10^{19} cm^{-3} or more, silicide is formed in the film with undesirable results.

[0025]

The step of forming the crystalline silicon film can consist of heat-treating it at a temperature of about 450 to 600°C. The heating diffuses the metal element. Concomitantly, the amorphous silicon film is grown laterally, thus forming the crystalline silicon film.

[0026]

In order to diffuse the metal element into the amorphous silicon film, the heating temperature must be 400°C or higher. The upper limit of the heating temperature is limited by the maximum allowable temperature of the substrate, i.e., its strain point. For example, where a glass substrate is employed, setting the heating temperature to about 550°C is appropriate from the viewpoint of the heat resistance of the glass substrate and the productivity. Where a substrate of a material withstanding a temperature of 1000°C or higher such as quartz substrate is used, the heating temperature can be elevated with increasing the maximum allowable temperature.

[0027]

The present invention is characterized in that the active layer can be formed by etching the crystalline silicon film without removing the first insulating film acting as a masking film; rather the first insulating film is left on the crystalline silicon film. Thus, the surface of the silicon film forming the active layer remains coated with the first insulating film during a time interval between the formation of the first insulating film and the completion of the semiconductor devices. Consequently, the surface is protected from contamination. The interface between the gate-insulating film and the active layer can exhibit good characteristics.

[0028]

After forming the active layer, the second insulating film is formed. As a result, the gate-insulating film consisting of the two layers, i.e., the first and second insulating films, is formed.

Therefore, the first and second insulating films may be made of silicon oxide or silicon nitride. However, the first insulating film is required to be so thick that it functions as a barrier film when a metal element is introduced. For example, where the first insulating film is formed from silicon oxide, a film thickness of several tens of angstroms is necessary. In practical, the film thickness is set to several hundreds of angstroms.

[0029]

To change the first insulating film into a thermal oxide film of silicon, an amorphous silicon film is thermally oxidized, thereby the characteristics of the interface between the active layer (crystalline silicon film) and the gate-insulating film (first insulating film) can be made better than those of the interface between the crystalline silicon and the CVD silicon oxide film. The thermal oxidization step can be performed by wet oxidation or hydrogen chloride oxidation. It is to be noted that the heating temperature, the heating time, and other conditions are required to be set in such a way that the amorphous silicon film is not crystallized and that the used substrate is not deformed.

[0030]

If a sufficient film thickness is not obtained by the thermal oxidation method, a silicon oxide film or silicon nitride film is deposited by chemical vapor deposition on the thermal oxide silicon film to impart a sufficient film thickness to the first insulating film.

[0031]

In the method of fabricating a semiconductor device according to the present invention, a laser irradiation step i.e., a laser annealing step can be performed after the step of forming the crystalline silicon film. This can improve the crystallinity of the crystalline silicon film. At this time, the first insulating film exists on the surface of the crystalline silicon film. This acts to suppress ridges generated by the laser annealing.

[0032]

Measurements with an AFM have revealed that where no capping layer existed as in the prior art techniques, the sizes of the ridges were about 500 Å, and that where a capping layer consisting of the silicon oxide film according to the invention existed, the sizes of the ridges were not more than about 200 Å. Generation of the ridges can be suppressed by subjecting the crystalline silicon film to laser annealing in a state where the first insulating film is laminated.

[0033]

In another feature of the invention, the first insulating layer acts not only as the capping layer for suppressing generation of the ridges but also as an antireflective film for laser light. This can more effectively supply the laser energy to the crystalline silicon.

[0034]

The laser irradiation induces multiple reflection at the interface between the first insulating film and the crystalline silicon film and, therefore, the reflectivity of the surface of the first insulating film depends on the thickness of the first insulating film. Consequently, energy can be more effectively given to the crystalline silicon film by appropriately setting the thickness of the first insulating film than where laser light is directly irradiated on the surface of the crystalline silicon film.

[0035]

More specifically, the intensities of light reflected from the silicon oxide and the silicon nitride (in air) were calculated. The light has a wavelength of 248 nm (a KrF excimer laser light). The results of calculation are shown in Fig. 5, where the thickness of silicon oxide film is plotted on the horizontal axis and the theoretical values of reflected light is plotted on the vertical axis. As can be seen from the graph of Fig. 5, the intensity of reflected light varies in a sinusoidal relation to the film thickness. Since the phase depends also on the wavelength of the illuminating light, a curve indicating the intensities of reflected light having a wavelength of 308 nm, for example, emitted by an XeCl excimer laser is substantially equal to a curve obtained by translating the aforementioned curve several tens of nanometers along the horizontal axis.

[0036]

The silicon oxide film and the silicon nitride film may be made to act as antireflective films by controlling the film thickness in such a way that the intensity of reflected light assumes its minimum value. However, if the first insulating film is too thick, the laser energy cannot sufficiently reach the crystalline silicon film and so satisfactory effects of laser annealing can not obtained. Furthermore, it is impossible that the first insulating film acts as the gate-insulating film.

[0037]

Where these considerations are taken into account, it can be seen from Fig. 5 that the thickness of the silicon oxide film should be set to about 300 to 500 Å and the thickness of the silicon nitride film be set to 250 to 400 Å with respect to the KrF excimer laser light. However, the intensities of light shown in Fig. 5 was obtained theoretically. The actual reflected light intensity varies, depending on the refractive index of the film and on the used laser. The thickness of the first insulating film consisting of silicon oxide film and silicon nitride film may be appropriately determined, taking these into consideration. For instance, in the case that a KrF excimer laser light having a wavelength of 248 nm is emitted, the

thicknesses of the silicon oxide film and the silicon nitride film are set to 300-600 Å and 250-500 Å, respectively. In the case that an XeCl excimer laser light having a wavelength of 308 nm is illuminated, the thicknesses of the silicon oxide film and the silicon nitride film are set to 400-700 Å and 350-600 Å, respectively.

[0038]

In the step of forming the crystalline silicon film, the heat-treatment diffuses the metal element into the amorphous silicon film and very shallowly into the first insulating film. In the present invention, the lamination of the first and second insulating films forms the gate-insulating film. Therefore, if the first insulating film is heavily doped with a metal element, then the characteristics of the gate-insulating film are deteriorated. For this reason, it is desired to remove the surface regions of the first insulating film which are heavily doped with the metal element.

[0039]

More specifically, the surface of the first insulating film is cleaned by a megasonic process or other means. Then, the surface is etched to a depth of several tens of angstroms to several hundreds of angstroms with diluted HF solution. The etched film thickness may be appropriately determined according to the quality of the first insulating film and the used metal. Furthermore, this step may be carried out after forming the crystalline silicon film. Where this step is effected before the laser annealing step, the etching may be performed in such a way that the first insulating film acts as an antireflective film.

[0040]

[Embodiment]

[Embodiment 1]

Figs. 1 and 2 are cross-sectional views illustrating the process sequence for fabricating a thin-film transistor (TFT) of the present example. In the present example, a silicon film is crystallized by using a solution containing nickel.

[0041]

As shown in Fig. 1(A), a silicon oxide film is formed as a base film 102 on a glass substrate 101 to a thickness of 3000 Å by sputtering techniques. Then, an amorphous silicon film 103 is formed on the base film to a thickness of 500 Å by plasma CVD or low pressure thermal CVD.

[0042]

The surface of the amorphous silicon film 103 is oxidized to form a thin oxide film (not shown) having a thickness of about 10 to 50 Å. This thin oxide film improves the surface characteristics of the amorphous silicon film 103. The silicon film 103 no longer repels aqueous

solution. In the present example, the laminate is illuminated with ultraviolet radiation in an oxygen ambient to form a thin oxide film (not shown) to a thickness of 20 Å.

[0043]

Then, a silicon oxide film 104 is formed to a thickness of 400 to 800 Å by plasma CVD or low pressure CVD. Preferably, the base film 102, the amorphous silicon film 103, and the silicon oxide film 104 are formed in succession. Because the interface between the amorphous silicon film 103 and the silicon oxide film 104 is retained as it is until the final TFT is completed, and because the characteristics of this interface affect the characteristics of the TFT, it is necessary to form the amorphous silicon film 103 and the silicon oxide film 104 with special care.

[0044]

After forming the silicon oxide film 104, a rectangular hole 104a extending normal to the plane of figure is formed by a well-known etching process. During this etching process, alignment markers which act as indicia after the formation of the active layer can be formed.

[0045]

The surface of the amorphous silicon film 103 which is exposed through the hole 104a in the silicon oxide film 104 is oxidized to form a thin oxide film (not shown) having a thickness of about 10 to 50 Å. This thin oxide film improves the surface characteristics of the amorphous silicon film 103 and thus the amorphous silicon film no longer repels water solution. In the present example, the film is illuminated with ultraviolet radiation within an oxygen atmosphere to form the thin oxide film (not shown) to a thickness of 20 Å.

[0046]

Under this condition, a solution containing nickel which is a metal element promoting crystallization of silicon is applied. In the present example, aqueous solution of nickel acetate containing 10 ppm nickel is applied by spin coating and dried to form an extremely thin nickel acetate film 105. At this time, a thin oxide film (not shown) is present on the surface of the amorphous silicon film 103 in the hole 104a. Since the film thickness is as small as 20 Å, the surface of the amorphous silicon film 103 is substantially exposed. Hence, nickel is held in contact with the surface of the amorphous silicon film 103 in the hole 104a formed in the silicon oxide film 104.

[0047]

As shown in Fig. 1(B), a heat-treatment is performed at 550°C for 8 hours in a nitrogen atmosphere. The thin nickel acetate film 105 is decomposed at 400°C, so that nickel element is diffused into the amorphous silicon film 103 through the hole 104a in the silicon oxide film 104. The amorphous silicon film 103 is crystallized laterally as indicated by the arrows, thus forming

a crystalline silicon film 106. As shown in Fig. 1(C), in a region 106a located immediately under the thin nickel acetate film 105, crystals have been grown vertically. In its surrounding region 106b, crystals have been grown laterally. This heat-treatment may be carried out at 450 to 600°C. Where a glass substrate is used, this heat-treatment temperature is preferably set below the strain point of the glass substrate to prevent the glass substrate from shrinking or deforming.

[0048]

Then, as shown in Fig. 1(C), laser annealing is performed without removing the silicon oxide film 104 to improve the crystallinity of the crystalline silicon film 16 further. In the present example, a KrF excimer laser (a wavelength of 248 nm) or an XeCl excimer laser having a wavelength of 304 nm is emitted. At this time, the silicon oxide film 104 is present on the surface of the crystalline silicon film 16 and so generation of ridges is suppressed. The thickness of the silicon oxide film 104 is set to 500 Å. The oxide film acts as an antireflective film for light having a wavelength of 248 nm as shown in Fig. 5. In consequence, laser energy can be efficiently given to the crystalline silicon film 106.

[0049]

Before the laser annealing step, the surface of the silicon oxide film 104 which is heavily doped with nickel may be removed to a depth of several tens of angstroms to several hundreds of angstroms. In this case, the surface is first cleaned by a megasonic process and etched with diluted HF solution. During the etching, the thickness of the silicon oxide film 104 is so set that the film acts as an antireflective film for laser light. Therefore, the thickness of the silicon oxide film 104 may be determined, taking account of the depth achieved by this etching step.

[0050]

As shown in Fig. 1(D), the crystalline silicon film 106 is etched into islands while the silicon oxide film 104 is laminated on the silicon film, thus forming an active layer 107. The etched silicon oxide film 104 acts as a gate-insulating film. After the end of the etching, a silicon oxide film 109 is formed to a thickness of 1000 Å by plasma CVD or low pressure CVD. These silicon oxide films 104 and 109 together form a gate-insulating film.

[0051]

In the present example, the lower layer of the gate-insulating film consists of the silicon oxide film 104. However, the lower layer may also consist of a silicon nitride film. In this case, the thickness of the silicon nitride film is controlled according to the wavelength of the laser light used during the laser annealing step so that this film acts as an antireflective film. Furthermore, instead of the silicon oxide film 109 as the upper layer of the gate-insulating film, a silicon nitride film may be deposited.

[0052]

After forming the silicon oxide film 109, an aluminum film having a thickness of 4000 Å is formed on the surface of the gate-insulating film 110 consisting of the silicon oxide films 104 and 109 by sputtering, as shown in Fig. 2(A). The aluminum film is patterned to form a gate electrode 111. Formation of hillocks and whiskers is prevented during heating steps and other later steps by previously adding 0.2% by weight of scandium to the aluminum.

[0053]

As shown in Fig. 2(B), an anodic oxide 112 having a thickness of 1500 to 2000 Å is formed around the gate electrode 111 by the anodization technique disclosed in Japanese Patent Laid-Open No. 267667/1993. In the present example, an electrolytic solution is prepared by neutralizing ethylene glycol solution containing 3% tartaric acid with aqueous ammonia to pH 6.9. Within this electrolytic solution, a voltage is applied, using the gate electrode 105 as an anode. As a result, the dense and firm anodic oxide 112 is formed around the gate electrode 111. The thickness of the anodic oxide 112 determines the length of offset and the thickness of the anodic oxide 112 can be controlled by the voltage applied to the gate electrode 111.

[0054]

As shown in Fig. 2(C), impurities are implanted into the active layer 107 by ion implantation techniques, using the gate electrode 111 and surrounding anodic oxide 112 as a mask. In order to fabricate a P-channel TFT, phosphorus is introduced. Using phosphine (PH_3) as a dopant gas, phosphorus ions are implanted. On the other hand, in order to fabricate an N-channel TFT, boron ions are introduced, using diborane (B_2H_6) as a dopant gas. As a result, a source region 113, a drain region 114, and a channel region 115 are formed in the active layer 107 by self-alignment manner.

[0055]

In the present example, the anodic oxide 112 is formed around the gate electrode 111. Therefore, the source region 113 and the drain region 114 are shifted from the ends of the gate electrode 111 by an amount equal to the thickness of the anodic oxide 112. That is, an offset structure can be formed. Since this offset structure acts as a high-resistivity region, the off current of the TFT can be reduced.

[0056]

As shown in Fig. 2(D), a silicon oxide film is formed as an interlayer insulator 116 to a thickness of 6000 Å by plasma CVD. The interlayer insulator 116 consists of a monolayer of silicon oxide. Instead, the interlayer insulator 116 can be made of a silicon nitride film or a multilayer film of silicon oxide and silicon nitride. The interlayer insulator 116 and the gate

insulating film 110 are etched to form contact holes in the source region 107 and in the drain region 108. A multilayer film of titanium and aluminum is formed over these contact holes and patterned to form upper wirings and electrodes, 117 and 118.

[0057]

Finally, the laminate is heat-treated at a temperature of 300°C in a hydrogen atmosphere, thus completing the TFT.

[0058]

In the present example, the surface of the active layer 107 (crystalline silicon film 106) is not exposed during a time interval between the instant when the silicon oxide 104 is formed and the instant when the TFT is completed. Therefore, the surface is prevented from getting contaminated. The layer can be made to act as a capping layer which suppresses formation of ridges that would normally be generated by laser annealing.

[0059]

Furthermore, the thickness of the silicon oxide 104 is so controlled that the layer acts as an antireflective film for the wavelength of the used laser light. In consequence, the laser energy can be effectively afforded to the film.

[0060]

[Embodiment 2]

Figs. 3 and 4 are cross-sectional views illustrating a process sequence for fabricating a TFT according to Embodiment 2. As shown in Fig. 3(A), a glass substrate 201 made of Corning 1737 or Corning 7059 is prepared, and a silicon oxide film is formed as a base film 202 on the substrate to a thickness of 1000 to 5000 Å, e.g., 1200 Å by sputtering. Then, an amorphous silicon film 203 is formed to a thickness of 500 Å by plasma CVD. Preferably, the base film 202 and the amorphous silicon film 203 are formed in succession.

[0061]

Subsequently, a silicon thermal oxide film 204 is formed on the surface of the amorphous silicon film 203 to a thickness of several tens of angstroms. The thermal oxidation conditions such as atmosphere and pressure may be appropriately selected. However, it is necessary to control the heating temperature and heating time in such a way that the amorphous silicon film 203 is not crystallized and that the glass substrate 201 is not deformed. The characteristics of the interface between the amorphous silicon film 203 and the silicon thermal oxide film 204 formed by this oxidation step are well maintained until the final TFT is obtained. Consequently, the characteristics of the TFT can be improved.

[0062]

Then, a silicon oxide film 205 is formed on the surface of the silicon thermal oxide film 204 by plasma CVD or low pressure CVD. The silicon thermal oxide film 204 and the silicon oxide film 205 together form a masking layer when a metal element is introduced. During laser annealing, they serve as an antireflective film for laser light. For these purposes, it is necessary to control the thickness of the lamination of the silicon thermal oxide film 204 and the silicon oxide film 205 according to the wavelength of the used laser light.

[0063]

As shown in Fig. 3(B), the silicon oxide film 205 and the silicon thermal oxide film 204 are etched to form a rectangular hole 206 whose longitudinal direction is a vertical direction to the drawing sheet. At this time, alignment markers used after the formation of the active layer can be formed.

[0064]

Then, the surface of the amorphous silicon film 203 which is exposed through the hole 206 in the silicon oxide film 205 is oxidized to form a thin oxide film (not shown) having a thickness of approximately 10 to 50 Å. This oxide film improves the surface characteristics of the amorphous silicon film 203. As a result, the film no longer repels aqueous solution. The thin oxide film can be formed by ultraviolet radiation within an oxygen atmosphere or immersing the substrate in ozone water or hydrogen peroxide water.

[0065]

Under this condition, a solution containing nickel which is a metal element promoting crystallization of silicon is applied. In the present example, aqueous solution containing 1 to 100 ppm of nickel acetate is applied by spin coating to form an extremely thin nickel acetate film 207. As a result, nickel is maintained in contact with the surface of the amorphous silicon film 203 in the hole 104a within the silicon oxide film 104

[0066]

As shown in Fig. 3(C), a heat-treatment is performed at 550°C for 8 hours in a nitrogen atmosphere. The thin nickel acetate film 207 is decomposed at 400°C, so that nickel element is diffused into the amorphous silicon film 203 through the hole 207. As the nickel element is diffused, the amorphous silicon film 203 is crystallized laterally as indicated by the arrows, thus forming a crystalline silicon film 208.

[0067]

As shown in Fig. 3(D), in a region 208a of the crystalline silicon film 208 located immediately under the hole 206, crystals have been grown vertically. In its surrounding region 208b, crystals have been grown laterally.

[0068]

As shown in Fig. 3(D), laser annealing is performed without removing the silicon thermal oxide film 204 or the silicon oxide film 205 to improve the crystallinity of the crystalline silicon film 208. In the present example, a KrF excimer laser (a wavelength of 248 nm) or an XeCl excimer laser (a wavelength of 304 nm) is emitted. At this time, on the surface of the crystalline silicon film 208, a capping layer consisting of the silicon thermal oxide film 204 and the silicon oxide film 205 is formed, thereby generation of ridges is suppressed Since the thickness of the lamination film of the silicon thermal oxide film 204 and the silicon oxide film 205 is set to 500 Å, the lamination film acts as an antireflective film for light having a wavelength of 248 nm, as shown in Fig. 5. Hence, the laser energy can be efficiently given to the crystalline silicon film 208.

[0069]

Before the laser annealing step, the surface of the silicon oxide film 205 which is heavily doped with nickel may be removed to a depth of several tens of angstroms to several hundreds of angstroms. In this case, the surface is first cleaned by a megasonic process and etched with diluted HF solution. The etching is conducted to a depth so that the lamination film of the silicon thermal oxide film 204 and the silicon oxide film 205 acts as an antireflective film for used laser light. Therefore, the thickness of the silicon oxide film 205 may be determined, taking account of the amount of the film removed by this etching step.

[0070]

Then, as shown in Fig. 3(E), the crystalline silicon film 208 is etched into islands while the silicon thermal oxide film 204 and the silicon oxide film 205 are laminated, thus forming an active layer 209. The etched lamination film of the silicon thermal oxide film 204 and the silicon oxide film 205 constitutes a gate-insulating film.

[0071]

As shown in Fig. 3(F), after the etching treatment is completed, a silicon oxide film 210 is formed to a thickness of 1000 Å by plasma CVD or low pressure CVD. These silicon thermal oxide film 204 and silicon oxide films 205, 210 together form the gate-insulating film.

[0072]

As shown in Fig. 4(A), an aluminum film for forming a gate electrode 212 is formed on the surface of a lamination film 211 consisting of the silicon thermal oxide film 204 and the silicon oxide films 205, 210 to a thickness of 5000 Å by sputtering techniques and patterned. Formation of hillocks and whiskers is prevented during heating steps and other later steps by previously adding 0.2% by weight of scandium to the aluminum.

[0073]

Then, the surface of the aluminum film is anodized to form an extremely thin, dense anodic oxide film 213. This is followed by formation of a resist mask 214 on the surface of the aluminum film. Since the dense anodic oxide 213 is present on the surface of the aluminum film, the resist mask 213 can be formed in intimate contact with the surface. Using the resist mask 214, the aluminum film is etched to form the gate electrode 212.

[0074]

As shown in Fig. 4(B), the gate electrode 212 is anodized while leaving the resist mask 214 behind. Thus, a porous anodic oxide 215 is formed on the side surfaces of the gate electrode 212 to a thickness of 4000 Å.

[0075]

As shown in Fig. 4(C), the resist mask 214 is peeled off. The gate electrode 212 is again anodized within an electrolytic solution to form a dense anodic oxide 216 to a thickness of 1000 Å.

[0076]

The anodic oxide can be formed differently by changing the used electrolytic solution. Where the porous anodic oxide 215 is formed, an acidic solution containing 3-20% citric acid, oxalic acid, chromic acid, or sulfuric acid is used as the electrolytic solution. On the other hand, where the dense anodic oxide 216 is formed, an electrolytic solution prepared by adjusting the pH of an ethylene glycol solution containing 3-10% tartaric acid, boric acid, or nitric acid to about 7 is used.

[0077]

As shown in Fig. 4(D), using the gate electrode 212, its surrounding porous anodic oxide 215, and the dense anodic oxide 216 as a mask, the lamination film 211 consisting of the silicon thermal oxide film 204 and silicon oxide films 205, 210 is etched to form a gate-insulating film 217.

[0078]

As shown in Fig. 4(E), the porous anodic oxide 215 is removed. Using the gate electrode 212, the dense anodic oxide 216, and the gate-insulating film 217 as a mask, impurities are implanted into the active layer 209 by ion implantation techniques. In the present example, where a P-channel TFT is formed, phosphine (PH_3) is used as a dopant gas in introducing phosphorus ions.

[0079]

In the ion implantation step, those regions which are not coated with the gate insulating film 217 are heavily doped with the dopant to form a source region 218 and a drain region 219 since

the gate insulating film 217 act as a semitransparent mask. In the regions masked only with the gate insulating film 217, lightly doped regions 220 and 221 are formed. Since no impurities are introduced into the region located immediately under the gate electrode 212, a channel region 222 is formed.

[0080]

Since the lightly doped regions 220 and 221 act as high-resistivity regions, they contribute to a decrease in the off current. The lightly doped region 221 on the side of the drain region 219 is termed an LDD (lightly doped drain) region. The region just under the dense anodic oxide 216 can be made to act as an offset region by making the dense anodic oxide 216 sufficiently thick. In this case, the off current can be reduced further.

[0081]

After the ion implantation step, a silicon oxide film is formed as an interlayer insulator 223 to a thickness of 5000 Å by plasma CVD, as shown in Fig. 4(F). Instead of the monolayer of silicon oxide, the interlayer insulator 223 may be made of a monolayer of silicon nitride or multilayer film of silicon oxide and silicon nitride.

[0082]

Then, the interlayer insulator 223 consisting of a silicon oxide film is etched by dry etching techniques to form contact holes in the source region 218 and the drain region 219. An aluminum film is formed over these contact holes to a thickness of 4000 Å by sputtering and etched to form an upper wirings and electrodes, 224 and 225.

[0083]

Finally, the laminate is heat-treated at a temperature of 350°C in a hydrogen atmosphere, thus completing the TFT.

[0084]

In the present embodiment, the surface of the active layer 209 (crystalline silicon film 208) is not exposed during a time interval between the instant when the silicon thermal oxide film 204 is formed and the instant when the TFT is completed.

[0085]

Further, in Embodiment 1, a silicon oxide film is formed on the surface of the active layer by CVD. In the present embodiment, a thermal oxide film is grown on the surface of the active layer 209. Consequently, the characteristics of the interface between the gate-insulating film and the active layer can be improved further. Hence, a TFT having better characteristics can be derived.

[0086]

Also in the present example, during the laser annealing, the lamination film of the silicon thermal oxide film 204 and the silicon oxide film 205 is made to act as a capping layer for suppressing formation of ridges. At the same time, the thickness of the lamination layer is so controlled that the layer serves as an antireflective film for the used laser light having a wavelength. Hence, the laser energy can be efficiently given to the crystalline silicon film 208.
[0087]

[Embodiment 3]

The present example is described by referring to Fig. 1. As shown in Fig. 1(A), a silicon oxide film is formed as a base film 102 on a glass substrate 101 to a thickness of 3000 Å by sputtering techniques. Then, an amorphous silicon film 103 is formed on the base film to a thickness of 500 Å by plasma CVD or low pressure thermal CVD.
[0088]

Then, a silicon oxide film 104 is formed by plasma CVD or low pressure CVD. Preferably, the base film 102, the amorphous silicon film 103, and the silicon oxide film 104 are formed in succession. Because the interface between the amorphous silicon film 103 and the silicon oxide film 104 is retained as it is until the final TFT is completed, and because the characteristics of this interface affect the characteristics of the TFT, it is necessary to form the amorphous silicon film 103 and the silicon oxide film 104 with special care.
[0089]

Then, a rectangular hole 104a extending normal to the plane of the figure is formed in the silicon oxide film 104 by a well-known etching process. During this etching process, alignment markers which act as mark after the formation of the active layer can be formed.
[0090]

The surface of the amorphous silicon film 103 which is exposed through the hole 104a in the silicon oxide film 104 is oxidized to form a thin oxide film (not shown) having a thickness of about 10 to 50 Å. This thin oxide film improves the surface characteristics of the amorphous silicon film 103 and thus the amorphous silicon film no longer repels water solution. The thin oxide film can be formed by ultraviolet radiation within an oxygen atmosphere or immersing the substrate in ozone water or hydrogen peroxide water.
[0091]

Then, aqueous solution containing 1 to 100 ppm of nickel acetate is applied by spin coating to form an extremely thin nickel acetate film 105. As a result, nickel is maintained in contact with the surface of the amorphous silicon film 103 in the hole 104a of the silicon oxide film 104.
[0092]

As shown in Fig. 1(B), a heat-treatment is performed at 550°C for 4 hours in a nitrogen atmosphere. The thin nickel acetate film 105 is decomposed at 400°C, so that nickel element is diffused into the amorphous silicon film 103 through the hole 104a in the silicon oxide film 104. At this time, the amorphous silicon film 103 is crystallized laterally as indicated by the arrows, thus forming a crystalline silicon film 106.

[0093]

As shown in Fig. 1(C), in a region 106a of the crystalline silicon film 106 that is located immediately under the thin nickel acetate film 105, crystals have been grown vertically. In its surrounding region 106b, crystals have been grown laterally.

[0094]

As shown in Fig. 1(D), the crystalline silicon film 106 is etched together with the silicon oxide film 104 to form an active layer 107. The etched silicon oxide film 104 acts as a gate-insulating film. After the end of the etching, a silicon oxide film 109 is formed to a thickness of 1000 Å by plasma CVD or low pressure CVD. These silicon oxide films 104 and 109 together form the gate-insulating film.

[0095]

Subsequently, the TFT is completed either by the TFT fabrication method of Embodiment 1 shown in Fig. 2 or by the TFT fabrication method of Embodiment 2 shown in Fig. 4.

[0096]

In the present embodiment, laser annealing is not performed after the crystallization step and, therefore, it is sufficient that the silicon oxide film 104 forming the bottom layer of the gate-insulating film has a thickness with which the silicon oxide film 104 acts as a barrier film when nickel acetate solution is applied. Furthermore, the silicon oxide film 104 may be formed by thermally oxidizing the amorphous silicon film 103. In this case, if the silicon oxide film 104 is not sufficiently thick, a silicon oxide film and a silicon nitride film may be deposited on the surface of the thermal oxide film to a desired total thickness by plasma CVD or low pressure CVD.

[0097]

In the present embodiment, the bottom layer of the gate-insulating film is made of the silicon oxide film 104. The bottom layer may also be made of a silicon nitride film. Furthermore, instead of the silicon oxide 109 forming the top layer of the gate-insulating film, a silicon nitride film may be deposited.

[0098]

In the present embodiment, the surface of the active layer 107 (crystalline silicon film 106) is not exposed during a time interval between the instant when the silicon oxide 104 is formed and

the instant when the TFT is completed. Therefore, the surface is prevented from getting contaminated. Furthermore, the layer (the barrier film) can be made to act as a capping layer which suppresses formation of ridges that would normally be generated by laser annealing.

[0099]

[Effect of the Invention]

In the method of fabricating a semiconductor device in accordance with the present invention, the first insulating layer forming the bottom layer of a gate-insulating film is made to act as a barrier film when a metal element is introduced into an amorphous silicon film. Even after a silicon film forming an active layer is crystallized, the surface is masked with the first insulating film and so the surface of the crystalline silicon film is prevented from being contaminated.

[0100]

Especially, if an amorphous silicon film is thermally oxidized such that the first insulating film is made of a silicon thermal oxide film, the characteristics of the interface between the active layer (crystalline silicon film) and the gate-insulating film (first insulating film) can be made better than those of the interface between the crystalline silicon and CVD silicon oxide film.

[0101]

In a further feature of the invention, laser annealing is performed while the first insulating film is left on the surface of the crystalline silicon. Consequently, formation of ridges can be suppressed. Moreover, the first insulating film can be used as an antireflective film for laser light by appropriately controlling the thickness of the first insulating film. Hence, the laser annealing can be carried out efficiently.

[Brief Description of Drawings]

Fig. 1 is a cross-sectional view illustrating a process sequence for fabricating a TFT according to Embodiment 1;

Fig. 2 is a cross-sectional view illustrating a process sequence for fabricating a TFT according to Embodiment 1;

Fig. 3 is a cross-sectional view illustrating a process sequence for fabricating a TFT according to Embodiment 2;

Fig. 4 is a cross-sectional view illustrating a process sequence for fabricating a TFT according to Embodiment 2;

Fig. 5 is a theoretical curve of intensities of reflected light having the wavelength of 248nm from the silicon oxide and the silicon nitride.

Fig. 6 is a cross sectional view illustrating a crystallization step of a conventional silicon

film.

[Description of Marks]
103 amorphous silicon film
104 silicon oxide film
105 thin nickel acetate film
106 crystalline silicon film
107 active layer
109 silicon oxide film
203 amorphous silicon film
204 silicon thermal oxide film
207 thin nickel acetate film
208 crystalline silicon film
209 active layer
210 silicon oxide film

[NAME OF DOCUMENT] Abstract

[PURPOSE]

The characteristics of the interface between the silicon film and the gate-insulating film can be improved by the catalytic action of a metal element.

[CONSTITUTION]

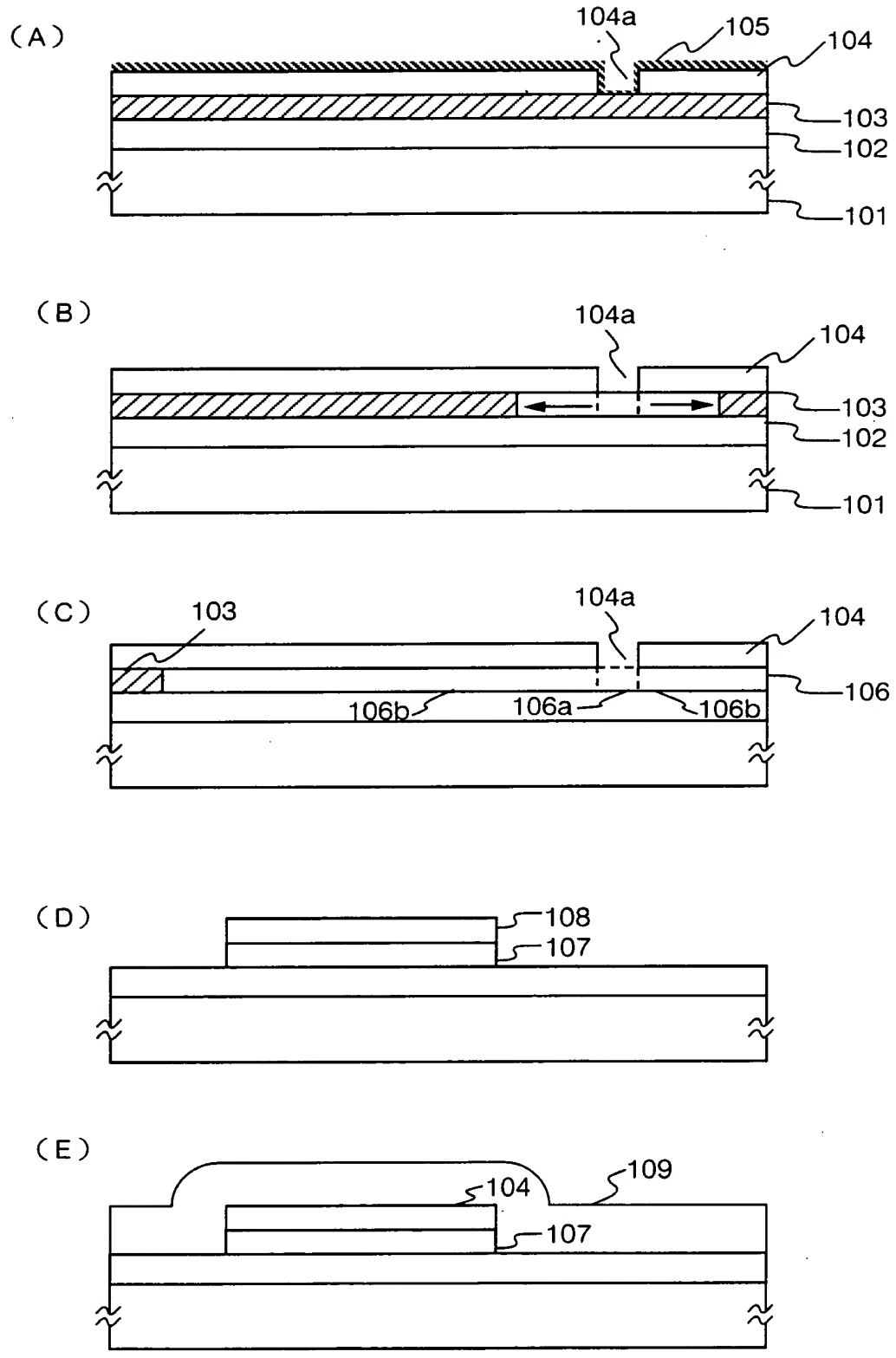
Nickel is selectively introduced into an amorphous silicon film 103 by a silicon oxide film 104 having a hole 104a and heat treatment is performed to form a crystalline silicon film 106. Further, the crystalline silicon film 106 is etched with a silicon oxide film 104 to form an active layer 107. The etched silicon oxide film 108 acts as a gate insulating film. After the crystallization step, by preventing the silicon oxide film 104 from being removed, the interface of the crystalline silicon film 106 can be kept fine.

[SELECTED DRAWING] Figure

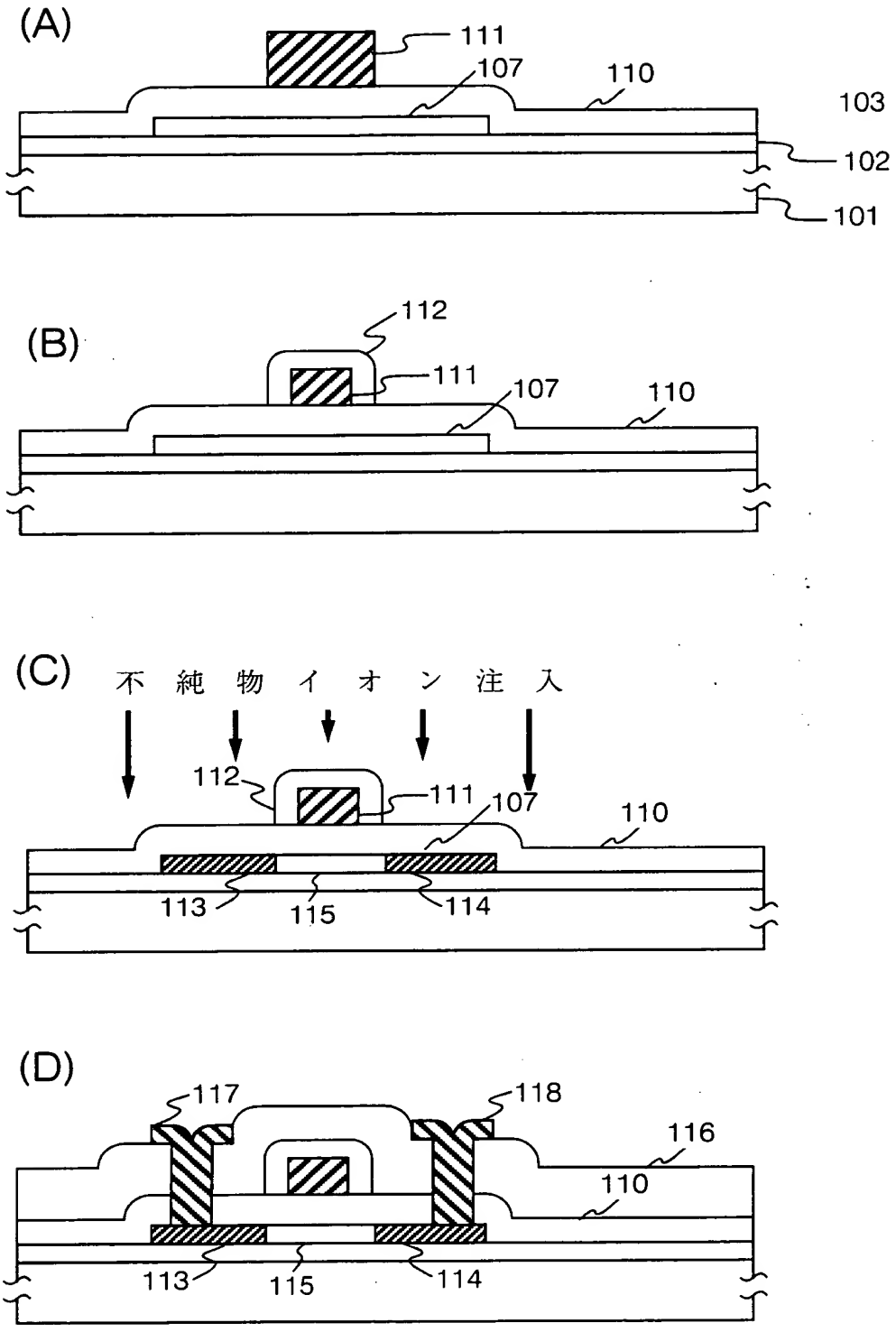
【整理番号】

【書類名】図面

【図１】



【図２】


(A)
111
107
110
103
102
101
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112
111
107
110
(C)
不 純 物 イ オ ン 注 入
112
111
107
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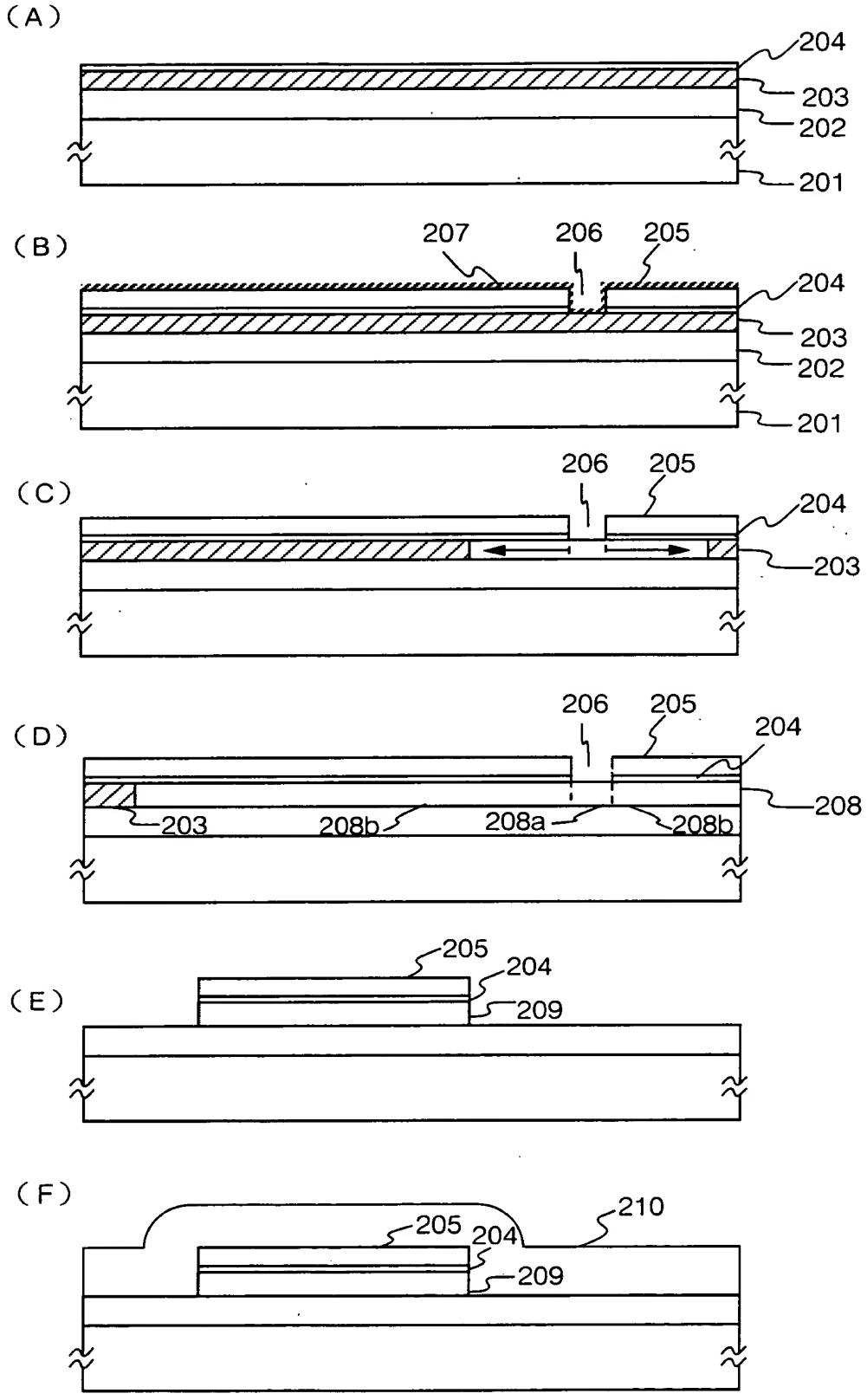
【図３】


（A）
204
203
202
201
（B）
207
206
205
204
203
202
201
（C）
206
205
204
203
（D）
206
205
204
208
203
208b
208a
208b
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205
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209
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210
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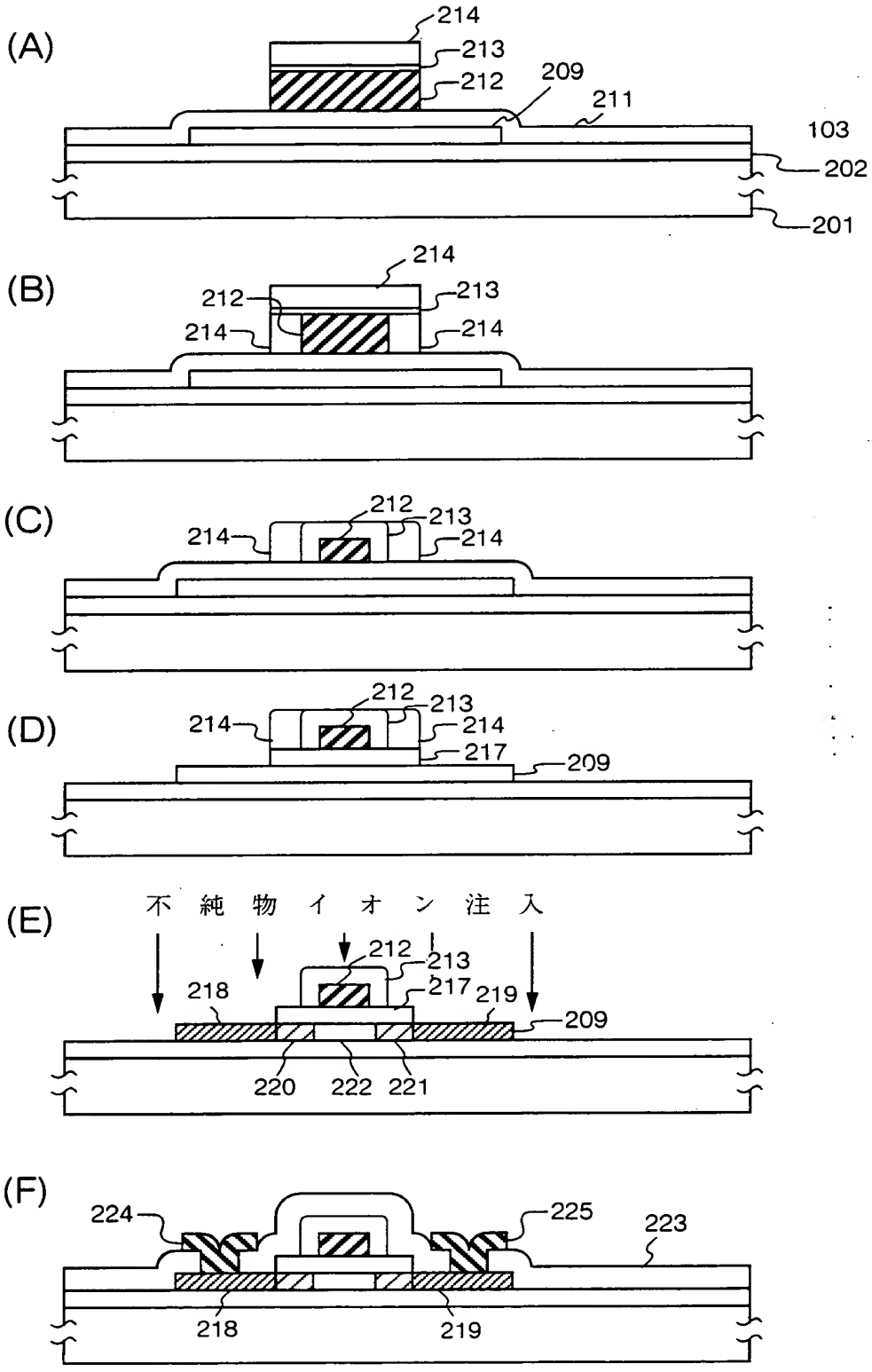
【図４】


(A)
214
213
212
209
211
103
202
201
(B)
214
212
213
214
214
(C)
212
213
214
214
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212
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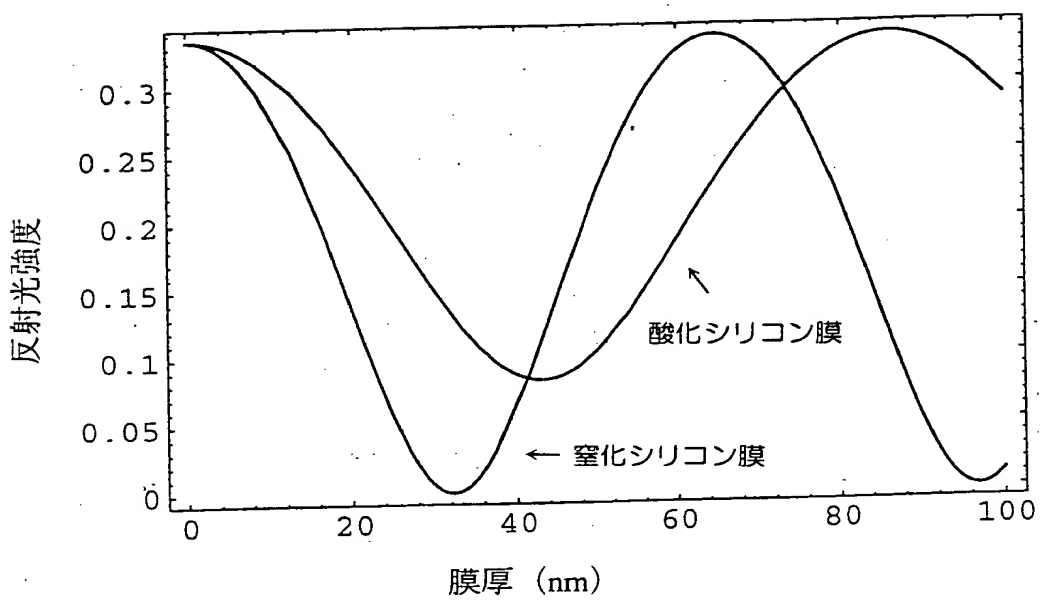
不 純 物 イ オ ン 注 入
212
213
218
217
219
209
220
222
221
(F)
224
225
223
218
219

【整理番号】

【図５】


反射光強度
0.3
0.25
0.2
0.15
0.1
0.05
0
0
20
40
60
80
100
膜厚（nm）
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【図６】